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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,944	MAZIASZ ET AL.	
	Examiner	Art Unit	
	PATRICK SANDOVAL	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-15 and 18-35, wherein claims 8 and 16-17 are cancelled* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-15 and 18-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Final Office Action responds to Applicant's amendment filed 1/20/2009. Claims 1, 18 and 28 have been amended and claims 8, 16 and 17 have been cancelled. Claims 1-7, 9-15 and 18-35 are pending.

Response to Arguments

2. Applicant's arguments and claim amendments filed 1/20/2009 have been fully considered but they are not persuasive. Applicable rejections are incorporated herein.

Claim Objections

3. **Claims 1-7, 9-15 and 18-35 are objected to** because the claimed invention is directed to non-statutory subject matter.

4. Claims 1, 18 and 28 are directed to non-statutory subject matter because a § 101 process claim must (1) be tied to another statutory class (a particular machine or apparatus) or (2) transform underlying subject matter (such as an article or materials) to a different state or thing; see In Re Bilski, 545 F.3d 943, 88 USPQ2d 1385 (Fed. Cir. 2008). If neither of these requirements are met by the claim, the method is not a patent eligible process under § 101.

5. A § 101 process claim that would not qualify as a statutory process would be a claim that recites purely mental step(s) that can be performed manually or merely manipulating an abstract idea without the use of a specific structure. Thus, to qualify as a § 101 statutory process, the claimed step(s) must explicitly recite the other statutory class such as machine (i.e., the computer, the thing) to which it is tied, for example by identifying the machine/computer that accomplishes the step(s) and providing

transformation underlying subject matter to a different state or thing to provide meaningful, reasonable limits and a practical application.

6. Claims 1, 18 and 28 recite a series of process steps for compacting a circuit layout but the steps neither explicitly recite a specific machine/computer that implements the claimed steps nor identify transformation of underlying subject matter to a different state or thing. As such, the subject matter of claims 1, 18 and 28 is non-statutory and not patent eligible.

7. Examiner suggests that in order to overcome objection, a limitation, i.e., "by using a computer" must be inserted in one of the claimed steps of claims 1, 18 and 28. This would overcome objection as long as the disclosure supports "a computer".

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. **Claims 1-7, 9-15 and 18-35 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. **Pursuant to independent claims 1, 18 and 28**, regarding the amended limitation "in response to determining the nonobject increasing operation/automated transistor width portion redistribution operation/object redistribution operation/automated object rotation operation d*oes not reduce the size of the critical path, restoring the circuit layout*", the following is unclear:

First, it is unclear as to how reduction of the size of the critical path is evaluated. Does this refer to a physical area reduction? Parameter reduction of a critical path?

Second, although the limitations disclose that when restoring the circuit layout given that the nonobject increasing operation/automated transistor width portion redistribution operation/object redistribution operation/automated object rotation operation d*oes not reduce the size of the critical path,* it is unclear as to what alternatively occurs given the nonobject increasing operation/automated transistor width portion redistribution operation/object redistribution operation/automated object rotation operation d*oes reduce the size of the critical path.*

Third, it is unclear as to what the circuit layout is restored to. Is a layout restored to a previous or original version? Restored to another modified version? Restored, in terms of being fixed to meet design constraints via modification of devices in a critical path?

11. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. **Claims 1-5, 7, 9, 10, 28-31, 33 and 34 are rejected** under 35 U.S.C. 102(b) as being anticipated by Markosian et al. (Markosian) (US 6,446,239).

14. **Pursuant to claim 1**, Markosian discloses a method of compacting a circuit layout comprising:

determining a critical path of a circuit layout (Markosian, Col. 3, ll. 31-67 – Col. 4, ll. 1-22);

performing an automated nonobject-increasing operation with respect to an object in the critical path for decreasing a size of the object in a direction of the critical path (Markosian, Col. 5, ll. 31-55, layout compaction); and

in response to determining the nonobject increasing operation does not reduce the size of the critical path, restoring the circuit layout (Markosian, Col. 5, ll. 45-52, wherein Markosian's cell compaction automatically moves/rotates/alters aspect ratios/changes shapes in an initial layout *provided an improvement in user configured design parameters results*, Col. 6, ll. 1-13 and Col. 6, ll. 60-67 - Col. 7, ll. 1-5, wherein user configured target design parameters such as power, timing and area are met/improved through compaction).

15. **Pursuant to claim 2,** Markosian discloses wherein the automated nonobject-increasing operation decreases the size of the object in the critical path by rotating the object (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

16. **Pursuant to claim 3,** Markosian discloses wherein the automated nonobject-increasing operation decreases the size of an object in the critical path by reshaping the

object (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes shape changes).

17. **Pursuant to claim 4,** Markosian discloses wherein the automated nonobject-increasing operation decreases the size of an object in the critical path by redistributing at least a portion of the object (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes redistribution by aspect ratio alterations).

18. **Pursuant to claim 5,** Markosian discloses wherein the performing the automated nonobject-increasing operation includes performing an object rotation operation on an object in the critical path (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

19. **Pursuant to claim 7,** Markosian discloses wherein the object rotation operation includes: rotating the object in the circuit layout (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

20. **Pursuant to claim 9,** Markosian discloses wherein object has a width in a first dimension and a width in a second dimension orthogonal to the first dimension, wherein the width in the first dimension is greater than the width in the second dimension, wherein the rotating includes rotating the object such that the second direction is parallel with a compaction direction of the automated nonobject-increasing operation (Markosian, Col. 5, ll. 31-55, Col. 15, ll. 25- 64, wherein layout compaction and rotation for cost minimization inherently includes rotating and compacting as necessary in order to meet predetermined timing and/or area costs for example).

21. **Pursuant to claim 10,** Markosian discloses wherein the performing the automated nonobject-increasing operation includes performing an object redistribution operation on an object in the critical path (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes redistribution by aspect ratio alterations).

22. **Pursuant to claim 28,** Markosian discloses a method of compacting a circuit layout comprising:

determining a critical path of a circuit layout (Markosian, Col. 3, ll. 31-67 – Col. 4, ll. 1-22);

performing at least one of an object redistribution operation on an object in the critical path (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes redistribution by aspect ratio alterations) and an automated object rotation operation on an object in the critical path for compacting the circuit layout (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation) ; and

in response to determining the object redistribution operation or the automated object rotation operation does not reduce the size of the critical path, restoring the circuit layout (Markosian, Col. 5, ll. 45-52, wherein Markosian's cell compaction automatically moves/rotates/alters aspect ratios/changes shapes in an initial layout *provided an improvement in user configured design parameters results*, Col. 6, ll. 1-13 and Col. 6, ll. 60-67 - Col. 7, ll. 1-5, wherein user configured target design parameters such as power, timing and area are met/improved through compaction).

23. **Pursuant to claim 29,** Markosian discloses wherein the performing further includes performing an object rotation operation on an object in the critical path (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

24. **Pursuant to claim 30,** Markosian discloses wherein the automated object rotation operation includes: rotating the object in the circuit layout (Markosian, Col. 5, ll. 31-55, wherein layout compaction includes rotation).

25. **Pursuant to claim 31,** Markosian discloses wherein the automated object rotation operation further comprises: determining whether the rotation of the object reduces the critical path (Markosian, Col. 13, ll. 41-67 – Col. 14, ll. 1-10, wherein critical paths are given cost factors such as area, netlist, power, timing, etc., Col. 15, ll. 25- 64, wherein by adjusting critical nodes and paths subsequent costs are adjusted and reduced).

26. **Pursuant to claim 33,** Markosian discloses wherein object has a width in a first dimension and a width in a second dimension orthogonal to the first dimension, wherein the width in the first dimension is greater than the width in the second dimension, wherein the rotating includes rotating the object such that the second direction is parallel with a compaction direction of the automated nonobject-increasing operation (Markosian, Col. 5, ll. 31-55, Col. 15, ll. 25- 64, wherein layout compaction and rotation for cost minimization inherently includes rotating and compacting as necessary in order to meet predetermined timing and/or area costs for example).

27. **Pursuant to claim 34,** Markosian discloses wherein the operation is a nonobject increasing operation (Markosian, Col. 5, ll. 31-55, wherein a layout is compacted).

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. **Claims 6 and 11 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii et al. (Fujii) (US 6,584,599).

30. **Pursuant to claims 6 and 11**, Markosian discloses all of the elements of claim 1, from which claims 6 and 11 depend.

31. Although Markosian discloses cell compaction and cell width redistribution on cells in a critical path, Markosian does not specifically disclose cell width redistribution wherein the cells are transistors (Claim 11) that include interconnect pads (Claim 6).

32. Fujii does disclose width modification of transistors to improve speed and power (Fujii, Col. 1, ll. 54-65), wherein Fujii's transistors include interconnect or contact pads (Fujii, Figs. 1-2).

33. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the width modification of transistors with the cell width redistribution of Markosian in order to achieve optimal driving speed and power consumption (Fujii, Col. 1, ll. 61-65).

34. **Claims 32 and 35 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii et al. (Fujii) (US 6,584,599).

35. **Pursuant to claims 32 and 35**, Markosian discloses all of the elements of claim 28, from which claims 32 and 35 depend.

36. Although Markosian discloses cell compaction and cell width redistribution on cells in a critical path, Markosian does not specifically disclose cell width redistribution wherein the cells are transistors (Claim 35) that include interconnect pads (Claim 32).

37. Fujii does disclose width modification of transistors to improve speed and power (Fujii, Col. 1, ll. 54-65), wherein Fujii's transistors include interconnect or contact pads (Fujii, Figs. 1-2).

38. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the width modification of transistors with the cell width redistribution of Markosian in order to achieve optimal driving speed and power consumption (Fujii, Col. 1, ll. 61-65).

39. **Claims 12-15 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii, further in view of Ganesh et al. (Ganesh) (US 6,823,500).

40. Pursuant to claims 12 and 15, Markosian in view of Fujii discloses all of the elements of claim 11, from which claims 12 and 15 depend.

41. Although Markosian in view of Fujii discloses transistor width redistribution, Markosian in view of Fujii does not disclose transistor width redistribution in terms of redistribution amongst other transistor fingers.

42. Ganesh does disclose transistor folding schemes and transistor re-legging wherein a device is folded into legs to comply with device width requirements (Ganesh) (Col. 7, ll. 11-67 – Col. 8, ll. 1-38, device-based legging folding scheme, re-legging).

43. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the invention of Ganesh in creating legs/fingers and redistributing transistor width to said legs/fingers in order to comply with size constraints and also preserve circuit topology regularity amongst stacked transistors (Ganesh, Col. 7, ll. 51-67).

44. **Pursuant to claim 13,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is part of a logical transistor of the circuit layout, wherein the transistor finger removing operation includes redistributing the transistor finger to at least one other transistor finger of the logical transistor (Ganesh, Col. 7, ll. 11-67 – Col. 8, ll. 1-38, re-legging, differential-legging).

45. **Pursuant to claim 14,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is located in a middle portion of a transistor chain of the circuit layout, wherein transistor finger removing operation further comprises: leaving a diffusion gap at a position in the transistor chain of the transistor finger being redistributed (Ganesh, Col. 12, ll. 14-67 – Col. 13, ll. –2, diffusion gap optimization, diffusion breaks and diffusion sharing).

46. **Claim 18 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii et al. (Fujii) (US 6,584,599).

47. Markosian discloses:

determining a critical path of a circuit layout (Markosian, Col. 3, ll. 31-67 – Col. 4, ll. 1-22);

performing an automated width-portion redistribution operation with respect to an object in the critical path for reducing the critical path (Markosian, Col. 5, ll. 31-55, layout compaction); and

in response to determining the automated transistor width portion redistribution operation does not reduce the size of the critical path, restoring the circuit layout (Markosian, Col. 5, ll. 45-52, wherein Markosian's cell compaction automatically moves/rotates/alters aspect ratios/changes shapes in an initial layout *provided an improvement in user configured design parameters results*, Col. 6, ll. 1-13 and Col. 6, ll. 60-67 - Col. 7, ll. 1-5, wherein user configured target design parameters such as power, timing and area are met/improved through compaction).

48. Although Markosian discloses cell compaction and cell width redistribution on cells in a critical path, Markosian does not specifically disclose cell width redistribution wherein the cells are transistors.

49. Fujii does disclose width modification of transistors to improve speed and power (Fujii, Col. 1, ll. 54-65).

50. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the width modification of transistors with the cell width redistribution of Markosian in order to achieve optimal driving speed and power consumption (Fujii, Col. 1, ll. 61-65).

51. **Claims 19-27 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Markosian in view of Fujii, further in view of Ganesh et al. (Ganesh) (US 6,823,500).

52. Pursuant to claims 19 and 27, Markosian in view of Fujii discloses all of the elements of claim 18, from which claims 19 and 27 depend.

53. Although Markosian in view of Fujii discloses transistor width redistribution, Markosian in view of Fujii does not disclose transistor width redistribution in terms of transistor finger creation and width redistribution amongst other transistor fingers.

54. Ganesh does disclose transistor folding schemes and transistor re-legging wherein a device is folded into legs or fingers to comply with device width requirements (Ganesh) (Col. 7, ll. 11-67 – Col. 8, ll. 1-38, device-based legging folding scheme, re-legging).

55. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to incorporate the invention of Ganesh in creating legs/fingers and redistributing transistor width to said legs/fingers in order to comply with size constraints and also preserve circuit topology regularity amongst stacked transistors (Ganesh, Col. 7, ll. 51-67).

56. **Pursuant to claim 19,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor width portion is a transistor finger of a logical transistor of the circuit layout, the automated transistor redistribution operation further includes: redistributing at least a portion of the transistor finger to at least one other transistor finger of the logical transistor (Ganesh, Col. 7, ll. 11-67 – Col. 8, ll. 1-38, re-legging, differential-legging).

57. **Pursuant to claim 20,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the redistributing further includes: redistributing the transistor finger to

at least one other transistor finger of the logical transistor (Ganesh, Col. 7, ll. 11-67 – Col. 8, ll. 1-38, re-legging, differential-legging).

58. **Pursuant to claim 21,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is located on the end of a transistor chain of the circuit layout (Ganesh, Col. 7, ll. 12-67, Fig. 7, device-based relegging of stacked devices wherein folded devices are part of a chain).

59. **Pursuant to claim 22,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is located in a middle portion of a transistor chain of the circuit layout, wherein transistor finger redistribution operation further comprises: leaving a diffusion gap at a position in the transistor chain of the transistor finger being redistributed (Ganesh, Col. 7, ll. 12-67, Fig. 7, device-based relegging of stacked devices wherein folded devices are part of a chain).

60. **Pursuant to claim 23,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger redistribution operation further includes redistributing a second transistor finger (Ganesh, Col. 8, ll. 6-38, wherein differential legging multiple legs or fingers of a device are redistributed).

61. **Pursuant to claim 24,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger and the second transistor finger are part of the same logical transistor of the circuit layout (Ganesh, Col. 8, ll. 6-38, wherein differential legging multiple legs or fingers of a device are redistributed).

62. **Pursuant to claim 25,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the transistor finger is part of a first logical transistor and the second

transistor finger is part of a second logical transistor (Ganesh, Col. 6, ll. 23-59, wherein transistors are assigned to clusters and folded, Col. 7, ll. 1-67, differential legging).

63. **Pursuant to claim 26,** Markosian in view of Fujii, further in view of Ganesh discloses wherein the redistributing at least a portion of the transistor finger to at least one other transistor finger further includes adding at least a portion of the at least a portion of the transistor finger to a transistor finger of the at least one transistor finger thereby increasing a width of the transistor finger of the at least one transistor finger, wherein the width of the transistor finger of the at least one transistor finger is in a direction generally parallel to a compaction direction of the automated transistor redistribution operation (Ganesh, Col. 8, ll. 6-38, wherein differential legging multiple legs of a device are redistributed to comply with width legging limits).

Remarks

64. Applicant argues that Markosian does not disclose "in response to determining the nonobject increasing operation/automated transistor width redistribution operation/object redistribution operation/automated object rotation operation does not reduce the size of the critical path, restoring the circuit layout". The Examiner is not persuaded.

65. Markosian discloses generating layout modification solutions wherein user configured target design parameters such as power, timing and area are met/improved for through compaction of components within critical paths (Markosian, Col. 3, ll. 31-46, Col. 6, ll. 1-13 and Col. 6, ll. 60-67 - Col. 7, ll. 1-5), wherein Markosian's cell compaction automatically moves/rotates/alters shapes in an initial layout *provided only if an*

improvement in user configured design parameters results (Markosian, Col. 5, ll. 45-52), and thus any layout modification *solutions that improve target parameters* are perceived as acceptable solutions for modification of an initial layout for a user to choose from (Markosian, Col. 6, ll. 1-13). Any layout modification solutions *that do not improve target parameters are inherently unacceptable solutions* for modification of an initial layout and thus are not presented to a user as viable solutions. Thus, unacceptable layout modification solutions along with their respective unacceptable layout modifications would be deleted, essentially restoring a circuit layout.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PATRICK SANDOVAL whose telephone number is

(571)272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/
Primary Examiner, Art Unit 2825

/Patrick Sandoval/
Examiner, Art Unit 2825